CLAIMS

What is claimed is:

1. A method for forming a heterojunction bipolar transistor, comprising:

forming a sub-collector layer;

forming a collector layer atop the sub-collector layer;

forming a base layer atop the collector layer;

forming an emitter layer atop the collector layer;

forming a cap layer atop the emitter layer, wherein the base layer comprises a different material than at least one of the emitter layer and the collector layer;

forming an etch mask atop the cap layer to expose a portion of the cap layer;

selectively etching the exposed portion of the cap layer to form a sidewall with a reentry feature and to expose a portion of the emitter layer;

selectively etching the exposed portion of the emitter layer to expose a portion of the base layer; and

forming metal contacts on the exposed portion of the base layer and the exposed portion of the cap layer.

2. The method of claim 1, wherein the reentry feature comprises an undercut profile.

3. The method of claim 1, wherein said forming an etch mask comprises:

depositing an etch masking layer atop the cap layer;

forming and patterning a photoresist layer atop the etch masking layer to expose a portion of the etch masking layer; and

etching the exposed portion of the etch masking layer to expose the portion of the cap layer.

4. The method of claim 1, wherein said selectively etching the exposed portion of the cap layer and said selectively etching the exposed portion of the emitter layer comprise wet etches.

5. The method of claim 1, herein the etch mask is selected from the group consisting nitride and InP.

6. The method of claim 5, wherein the cap layer comprises InGaAs.

7. The method of claim 6, wherein the emitter layer is selected from the group consisting InP and AlInAs.

8. The method of claim 7, wherein the base layer is selected from the group consisting InGaAs and GaAsSb, the collector layer is selected from the group consisting InGaAs and InP, and the sub-collector layer comprises InP.

9. The method of claim 1, after said selectively etching the exposed portion of the emitter layer and prior to said forming metal contacts, further comprising:

forming a second etch mask atop the exposed portion of the base layer to expose a second portion of the base layer; and

selectively etching the second exposed portion of the base layer to form a second sidewall and to expose a portion of the collector layer.

10. The method of claim 9, further comprising selectively etching the exposed portion of the collector layer to form a third sidewall and to expose a portion of the sub-collector layer, wherein at least one of the second sidewall and the third sidewalls forms a second reentry feature.

11. The method of claim 10, further comprising forming a metal contact on the exposed portion of the sub-collector layer, wherein said forming metal contacts on the exposed portion of the base layer and the exposed portion of the cap layer and said forming a metal contact on the exposed portion of the sub-collector layer comprises a single metal deposition.

12. The method of claim 11, wherein said selectively etching the exposed portion of the base layer and said selectively etching the exposed portion of the collector layer comprise wet etches.

13. The method of claim 9, wherein the second etch mask is selected from the group consisting nitride and InP.

14. A heterojunction bipolar transistor, comprising:

a sub-collector;

a collector atop the sub-collector;

a base atop the collector;

a base contact atop the base;

an emitter atop the base;

an emitter cap atop the emitter, the emitter cap comprising a sidewall with a reentry feature; and

an emitter metal atop the emitter cap.

15. The transistor of claim 14, wherein the reentry feature comprises an undercut profile.

16. The transistor of claim 14, wherein at least one of the base and the collector comprises a second sidewall with a second reentry feature.

17. The transistor of claim 16, wherein the second reentry feature comprises an undercut profile.